

# DATA SHEET

## **TDA8763**

10-bit high-speed low-power  
analog-to-digital converter

Objective specification  
File under Integrated Circuits, IC02

1995 Apr 27

**Philips Semiconductors**



**PHILIPS**

# 10-bit high-speed low-power analog-to-digital converter

## TDA8763

### FEATURES

- 10-bit resolution
- Sampling rate up to 40 MHz
- DC sampling allowed
- One clock cycle conversion only
- High signal-to-noise ratio over a large analog input frequency range (9.3 effective bits at 4.43 MHz full-scale input at  $f_{\text{clk}} = 40$  MHz)
- No missing codes guaranteed
- In range (IR) 3-state TTL output
- TTL compatible digital inputs
- 3 to 5 V CMOS outputs
- Low-level AC clock input signal allowed
- Internal reference voltage regulator (external reference allowed)
- Power dissipation only 235 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample-and-hold circuit required.

### APPLICATIONS

High-speed analog-to-digital conversion for:

- Video data digitizing
- Radar pulse analysis
- Transient signal analysis
- High energy physics research
- $\Sigma\Delta$  modulators
- Medical imaging.

### GENERAL DESCRIPTION

The TDA8763 is a 10-bit high-speed low-power analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 10-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CCA}}$	analog supply voltage		4.75	5.0	5.25	V
$V_{\text{CCD}}$	digital supply voltage		4.75	5.0	5.25	V
$V_{\text{CCO}}$	output stages supply voltage		3.0	5.0	5.25	V
$I_{\text{CCA}}$	analog supply current		–	27	tbf	mA
$I_{\text{CCD}}$	digital supply current		–	16	tbf	mA
$I_{\text{CCO}}$	output stages supply current	$f_{\text{clk}} = 40$ MHz; ramp input	–	4	tbf	mA
INL	DC integral non-linearity		–	$\pm 0.8$	tbf	LSB
DNL	DC differential non-linearity		–	$\pm 0.5$	$\pm 0.9$	LSB
AINL	AC integral non-linearity	note 1	–	$\pm 1.0$	$\pm 2.0$	LSB
$f_{\text{clk(max)}}$	maximum clock frequency					
	TDA8763M/2		20	–	–	MHz
	TDA8763M/4		40	–	–	MHz
$P_{\text{tot}}$	total power dissipation	$f_{\text{clk}} = 40$ MHz; ramp input	–	235	tbf	mW

### Note

1. Full-scale sine wave ( $f_1 = 4.43$  MHz;  $f_{\text{clk}} = 40$  MHz).



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PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	clock input
$\overline{TC}$	2	two's complement input (active LOW)
V <sub>CCA</sub>	3	analog supply voltage (5 V)
AGND	4	analog ground
DEC	5	decoupling input
V <sub>RB</sub>	6	reference voltage BOTTOM input
V <sub>RM</sub>	7	reference voltage MIDDLE
V <sub>I</sub>	8	analog input voltage
V <sub>RT</sub>	9	reference voltage TOP input
$\overline{CE}$	10	chip enable input (TTL level input, active LOW)
V <sub>CCD2</sub>	11	digital supply voltage 2 (5 V)
DGND2	12	digital ground 2
V <sub>CCO</sub>	13	supply voltage for output stages (5 V)
OGND	14	output ground
n.c.	15	not connected
D0	16	data output; bit 0 (LSB)
D1	17	data output; bit 1
D2	18	data output; bit 2
D3	19	data output; bit 3
D4	20	data output; bit 4
D5	21	data output; bit 5
D6	22	data output; bit 6
D7	23	data output; bit 7
D8	24	data output; bit 8
D9	25	data output; bit 9 (MSB)
IR	26	in range data output
DGND1	27	digital ground 1
V <sub>CCD1</sub>	28	digital supply voltage 1 (5 V)

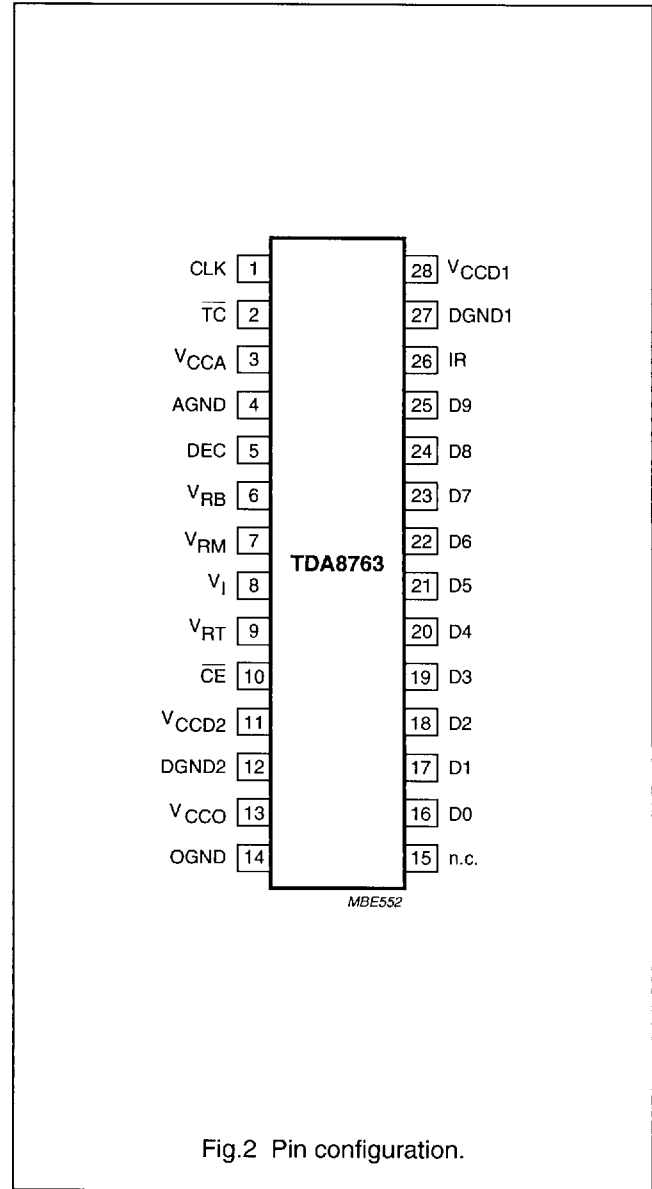


Fig.2 Pin configuration.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	note 1	-0.3	+7.0	V
$V_{CCD}$	digital supply voltage	note 1	-0.3	+7.0	V
$V_{CCO}$	output stages supply voltage	note 1	-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage difference				
	$V_{CCA} - V_{CCD}$		-1.0	+1.0	V
	$V_{CCA} - V_{CCO}$		-1.0	+4.0	V
	$V_{CCD} - V_{DDO}$		-1.0	+4.0	V
$V_I$	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	-	$V_{CCD}$	V
$I_O$	output current		-	10	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		0	+70	°C
$T_J$	junction temperature		-	+150	°C

### Note

- The supply voltages  $V_{CCA}$ ,  $V_{CCD}$  and  $V_{CCO}$  may have any value between -0.3 V and +7.0 V provided that the supply voltage differences between  $\Delta V_{CC}$  are respected.

## HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th j-a}$	thermal resistance from junction to ambient in free air	110	K/W

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**CHARACTERISTICS**

$V_{CCA} = V_3$  to  $V_4 = 4.75$  to  $5.25$  V;  $V_{CCD} = V_{11}$  to  $V_{12}$  and  $V_{28}$  to  $V_{27} = 4.75$  to  $5.25$  V;  $V_{CCO} = V_{13}$  to  $V_{14} = 4.4$  to  $5.25$  V; AGND and DGND shorted together;  $T_{amb} = 0$  to  $+70$  °C; typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 5$  V;  $V_{I(p-p)} = 2.0$  V;  $C_L = 15$  pF and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CCA}$	analog supply voltage		4.75	5.0	5.25	V
$V_{CCD1}$	digital supply voltage 1		4.75	5.0	5.25	V
$V_{CCD2}$	digital supply voltage 2		4.75	5.0	5.25	V
$V_{CCO}$	output stages supply voltage		3.0	5.0	5.25	V
$\Delta V_{CC}$	voltage difference					
	$V_{CCA} - V_{CCD}$		-0.20	-	+0.20	V
	$V_{CCA} - V_{CCO}$		-0.20	-	+2.25	V
	$V_{CCD} - V_{CCO}$		-0.20	-	+2.25	V
$I_{CCA}$	analog supply current		-	27	tbf	mA
$I_{CCD}$	digital supply current		-	16	tbf	mA
$I_{CCO}$	output stages supply current	$f_{clk} = 40$ MHz; ramp input	-	4	tbf	mA
<b>Inputs</b>						
CLOCK INPUT CLK (REFERENCED TO DGND); note 1						
$V_{IL}$	LOW level input voltage		0	-	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	-	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{clk} = 0.4$ V	-1	0	+1	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{clk} = 2.7$ V	-	-	20	$\mu$ A
$Z_I$	input impedance	$f_{clk} = 40$ MHz	-	2	-	k $\Omega$
$C_I$	input capacitance	$f_{clk} = 40$ MHz	-	2	-	pF
INPUT $\overline{CE}$ (REFERENCED TO DGND); see Table 2						
$V_{IL}$	LOW level input voltage		0	-	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	-	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{IL} = 0.4$ V	-1	-	-	$\mu$ A
$I_{IH}$	HIGH level input current	$V_{IH} = 2.7$ V	-	-	1	$\mu$ A
$V_I$ (ANALOG INPUT VOLTAGE REFERENCED TO AGND)						
$I_{IL}$	LOW level input current	$V_I = 1.3$ V	-	0	-	$\mu$ A
$I_{IH}$	HIGH level input current	$V_I = 3.8$ V	-	35	-	$\mu$ A
$Z_I$	input impedance	$f_i = 4.43$ MHz	-	7	-	k $\Omega$
$C_I$	input capacitance	$f_i = 4.43$ MHz	-	6	-	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Reference voltages for the resistor ladder using the internal voltage regulator; see Table 1</b>						
$V_{RB}$	reference voltage BOTTOM		tbf	1.3	–	V
$V_{RT}$	reference voltage TOP		–	3.8	tbf	V
$V_{diff}$	differential reference voltage $V_{RT} - V_{RB}$		tbf	2.5	tbf	V
$I_{ref}$	reference current		–	10	–	mA
$R_{LAD}$	resistor ladder		–	250	–	$\Omega$
$TC_{RLAD}$	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	158	–	m $\Omega$ /K
$V_{osB}$	offset voltage BOTTOM	note 2	–	250	–	mV
$V_{osT}$	offset voltage TOP	note 2	–	250	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	note 3	tbf	2.0	tbf	V
<b>Reference voltages for the resistor ladder using the external voltage regulator; see Table 1</b>						
$V_{RB}$	reference voltage BOTTOM		1.2	1.3	–	V
$V_{RT}$	reference voltage TOP		–	3.8	$V_{CCA} - 0.8$	V
$V_{diff}$	differential reference voltage $V_{RT} - V_{RB}$		1.8	2.5	3.0	V
$I_{ref}$	reference current		–	10	–	mA
$R_{LAD}$	resistor ladder		–	250	–	$\Omega$
$TC_{RLAD}$	temperature coefficient of the resistor ladder		–	1860	–	ppm
			–	158	–	m $\Omega$ /K
$V_{osB}$	offset voltage BOTTOM	note 2	–	250	–	mV
$V_{osT}$	offset voltage TOP	note 2	–	250	–	mV
$V_{I(p-p)}$	analog input voltage (peak-to-peak value)	note 3	1.5	2.0	2.5	V
<b>Outputs</b>						
DIGITAL OUTPUTS D9 TO D0 AND IR (REFERENCED TO OGND)						
$V_{OL}$	LOW level output voltage	$I_O = 1$ mA	0	–	0.4	V
$V_{OH}$	HIGH level output voltage	$I_O = -0.4$ mA	2.4	–	$V_{CCO}$	V
$I_{OZ}$	output current in 3-state mode	$0.4$ V < $V_O$ < $V_{CCO}$	–20	–	+20	$\mu$ A
<b>Switching characteristics</b>						
CLOCK INPUT CLK; see Fig.3; note 1						
$f_{clk(max)}$	maximum clock frequency TDA8763/2 TDA8763/4		20	–	–	MHz
			40	–	–	MHz
$t_{CPH}$	clock pulse width HIGH		8	–	–	ns
$t_{CPL}$	clock pulse width LOW		8	–	–	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog signal processing</b>						
LINEARITY						
INL	DC integral non-linearity		–	±0.8	tbf	LSB
DNL	DC differential non-linearity		–	±0.5	±0.9	LSB
AINL	AC integral non-linearity	note 4	–	±1.0	±2.0	LSB
OFER	offset error	middle code; $V_{RB} = 1.3 \text{ V}$ ; $V_{RT} = 3.8 \text{ V}$	–	±1	–	LSB
GER	gain error (from device to device) using external reference voltage	$V_{RB} = 1.3 \text{ V}$ ; $V_{RT} = 3.8 \text{ V}$ ; note 5	–	±0.1	–	%
	gain error (from device to device) using internal reference voltage	$V_{RB} = 1.3 \text{ V}$ ; $V_{RT} = 3.8 \text{ V}$ ; note 5	–	tbf	–	%
BANDWIDTH ( $f_{clk} = 40 \text{ MHz}$ )						
B	analog bandwidth	full-scale sine wave; note 6	–	tbf	–	MHz
		75% full-scale sine wave; note 6	–	tbf	–	MHz
		small signal at mid-scale; $V_I = \pm 10 \text{ LSB}$ at code 512; note 6	–	tbf	–	MHz
$t_{STLH}$	analog input settling time LOW-to-HIGH	full-scale square wave; see Fig.5; note 7	–	2.0	tbf	ns
$t_{STHL}$	analog input settling time HIGH-to-LOW	full-scale square wave; see Fig.5; note 7	–	2.5	tbf	ns
HARMONICS ( $f_{clk} = 40 \text{ MHz}$ )						
$h_1$	fundamental harmonics (full scale)	$f_i = 4.43 \text{ MHz}$	–	–	0	dB
$h_{all}$	harmonics (full scale); all components	$f_i = 4.43 \text{ MHz}$				
	second harmonics		–	–73	tbf	dB
	third harmonics		–	–70	tbf	dB
THD	total harmonic distortion	$f_i = 4.43 \text{ MHz}$	–	–68	–	dB
SIGNAL-TO-NOISE RATIO; note 8						
S/N	signal-to-noise ratio (full scale)	without harmonics; $f_{clk} = 40 \text{ MHz}$ ; $f_i = 4.43 \text{ MHz}$	56	58	–	dB



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
EFFECTIVE BITS; note 8						
EB	effective bits TDA8763M/2	$f_{\text{clk}} = 20 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.4	–	bits
EB	effective bits TDA8763M/4	$f_{\text{clk}} = 40 \text{ MHz}$				
		$f_i = 4.43 \text{ MHz}$	–	9.3	–	bits
		$f_i = 7.5 \text{ MHz}$	–	9.0	–	bits
		$f_i = 10 \text{ MHz}$	–	8.8	–	bits
		$f_i = 15 \text{ MHz}$	–	8.3	–	bits
TWO-TONE; note 9						
TTIR	two-tone intermodulation rejection	$f_{\text{clk}} = 40 \text{ MHz}$	–	–68	–	dB
BIT ERROR RATE						
BER	bit error rate	$f_{\text{clk}} = 40 \text{ MHz};$ $f_i = 4.43 \text{ MHz};$ $V_i = \pm 16 \text{ LSB}$ at code 512	–	tbf	–	times/ sample
DIFFERENTIAL GAIN; note 10						
$G_{\text{diff}}$	differential gain	$f_{\text{clk}} = 40 \text{ MHz};$ PAL modulated ramp	–	tbf	–	%
DIFFERENTIAL PHASE; note 10						
$\Phi_{\text{diff}}$	differential phase	$f_{\text{clk}} = 40 \text{ MHz};$ PAL modulated ramp	–	tbf	–	deg
<b>Timing (<math>f_{\text{clk}} = 40 \text{ MHz}; C_L = 15 \text{ pF}</math>); see Fig.3; note 11</b>						
$t_{\text{ds}}$	sampling delay time		–	–	2	ns
$t_{\text{h}}$	output hold time		5	–	–	ns
$t_{\text{d}}$	output delay time		–	10	14	ns
$C_L$	digital output load capacitance		–	15	40	pF
<b>3-state output delay times; see Fig.4</b>						
$t_{\text{dZH}}$	enable HIGH		–	tbf	tbf	ns
$t_{\text{dZL}}$	enable LOW		–	tbf	tbf	ns
$t_{\text{dHZ}}$	disable HIGH		–	tbf	tbf	ns
$t_{\text{dLZ}}$	disable LOW		–	tbf	tbf	ns

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## Notes to the characteristics

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 0.5 ns.
2. Analog input voltages producing code 0 up to and including code 1023:
  - a)  $V_{osB}$  (voltage offset BOTTOM) is the difference between the analog input which produces data equal to 00 and the reference voltage BOTTOM ( $V_{RB}$ ) at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
  - b)  $V_{osT}$  (voltage offset TOP) is the difference between  $V_{RT}$  (reference voltage TOP) and the analog input which produces data outputs equal to code 1023 at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
3. Analog input voltage range can be derived from  $V_{RT} - V_{RB}$  difference. It is  $\frac{(V_{RT} - V_{RB}) \times 8}{9}$
4. Full-scale sine wave ( $f_1 = 4.43\text{ MHz}$ ;  $f_{clk} = 40\text{ MHz}$ ).
5. 
$$GER = \frac{(V_{1023} - V_0) - 2\text{ V}}{2\text{ V}} \times 100$$
6. The analog bandwidth is defined as the maximum input sine wave frequency which can be applied to the device. No glitches greater than 2 LSBs, neither any significant attenuation are observed in the reconstructed signal.
7. The analog input settling time is the minimum time required for the input signal to be stabilized after a sharp full-scale input (square-wave signal) in order to sample the signal and obtain correct output data.
8. Effective bits are obtained via a Fast Fourier Transform (FFT) treatment taking 8K acquisition points per equivalent fundamental period. The calculation takes into account all harmonics and noise up to half of the clock frequency (NYQUIST frequency). Conversion to signal-to-noise ratio:  $S/N = EB \times 6.02 + 1.76\text{ dB}$ .
9. Intermodulation measured relative to either tone with analog input frequencies of 4.43 MHz and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full scale to the converter.
10. Measurement carried out using video analyser VM700A, where the video analog signal is reconstructed through a digital-to-analog converter.
11. Output data acquisition: the output data is available after the maximum delay time of  $t_d$ .

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**Table 1** Output coding and input voltage (typical values; referenced to AGND,  $V_{RB} = 1.3\text{ V}$ ,  $V_{RT} = 3.8\text{ V}$ )

STEP	$V_{I(p-p)}$	IR	BINARY OUTPUT BITS										TWO'S COMPLEMENT OUTPUT BITS										
			D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
U/F	<1.55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1.55	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	.	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
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1022	.	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0	
1023	3.55	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
O/F	>3.55	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	

**Table 2** Mode selection

$\overline{TC}$	$\overline{CE}$	D9 TO D0	IR
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

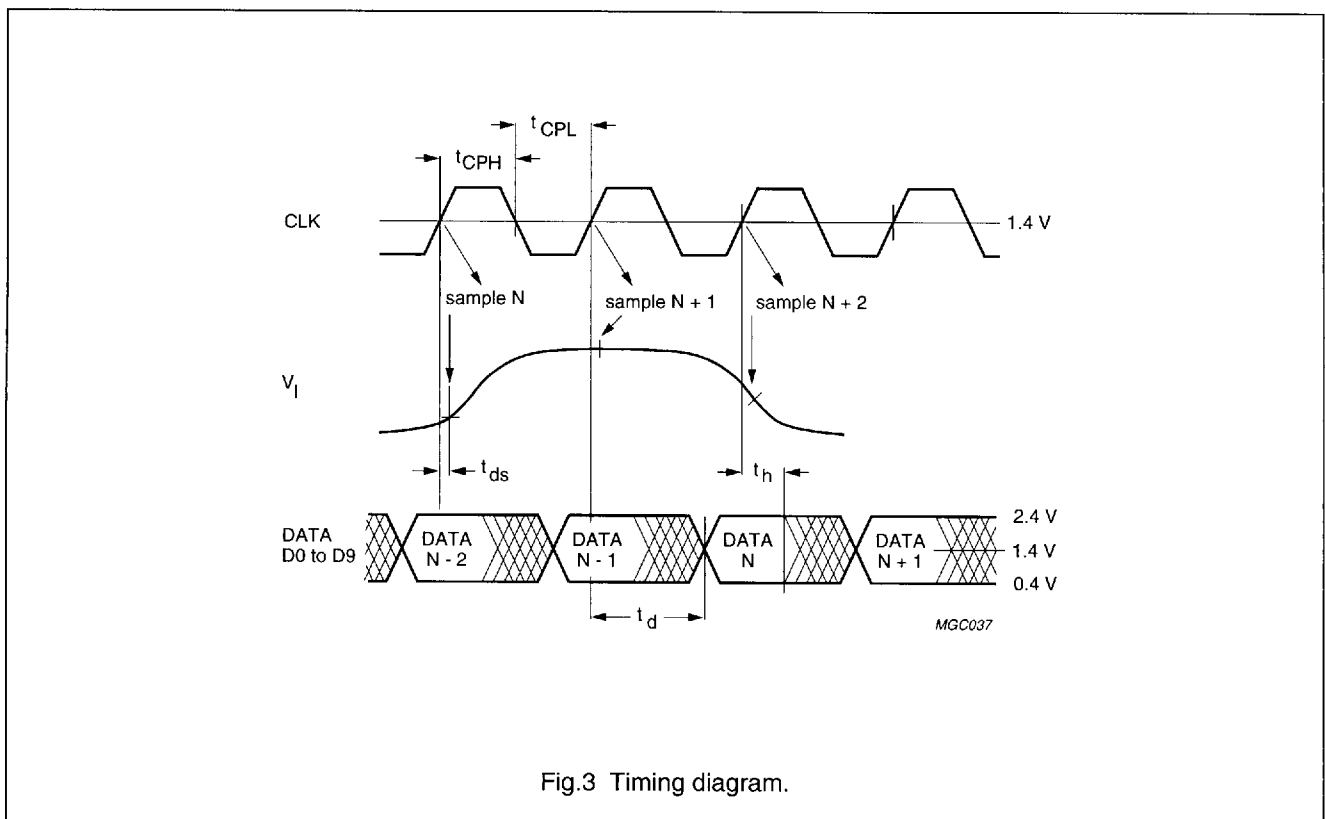
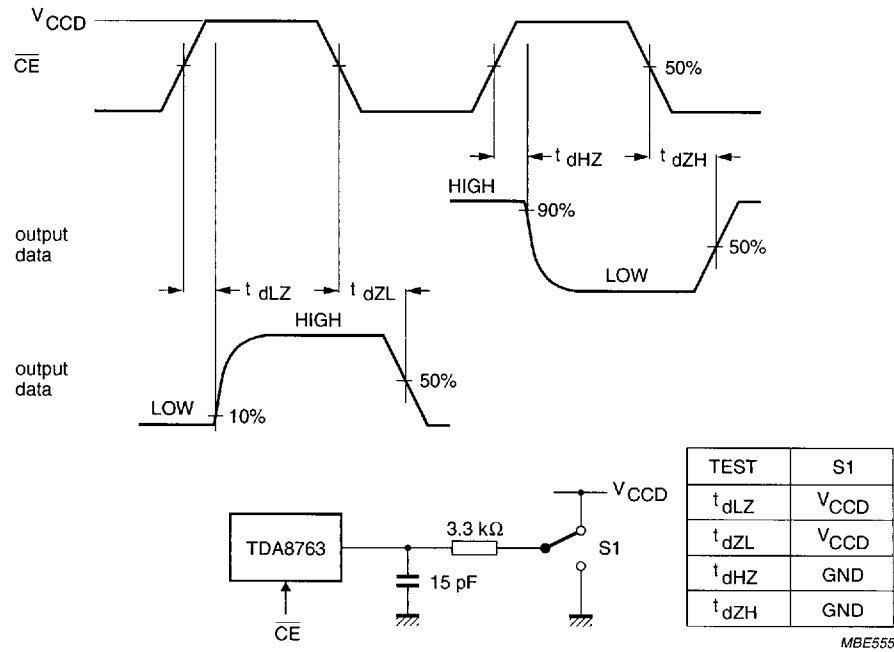


Fig.3 Timing diagram.

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$f_{\overline{CE}} = 100$  kHz.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

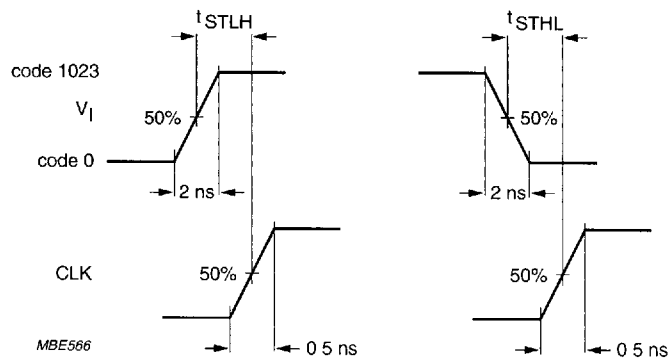


Fig.5 Analog input settling-time diagram.

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### INTERNAL PIN CONFIGURATIONS

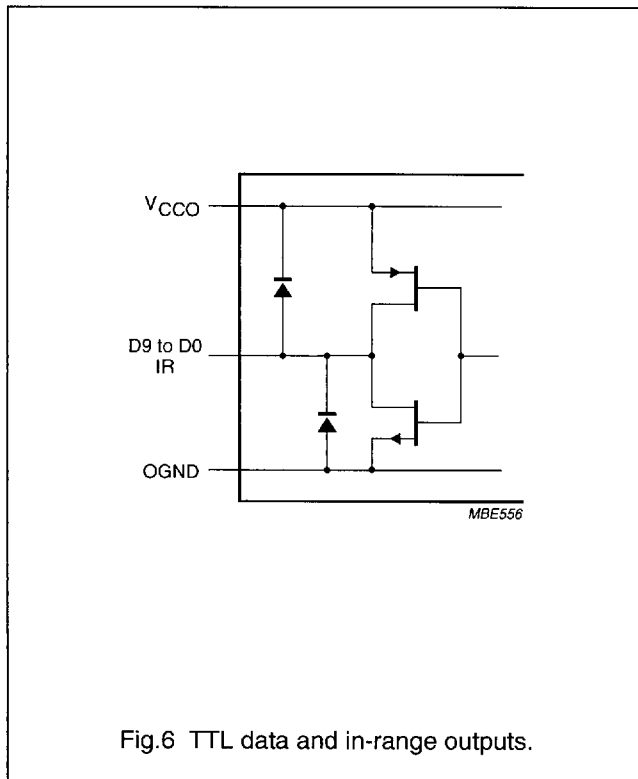


Fig.6 TTL data and in-range outputs.

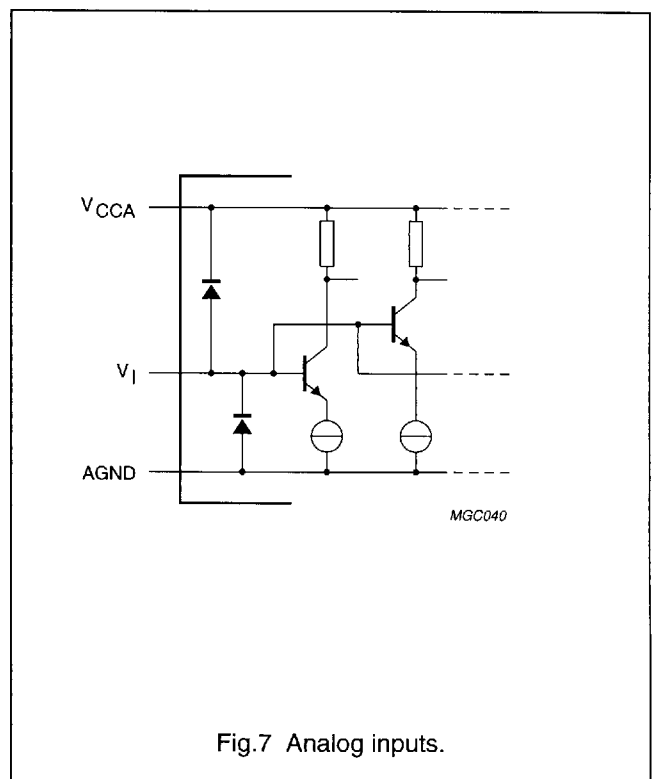


Fig.7 Analog inputs.

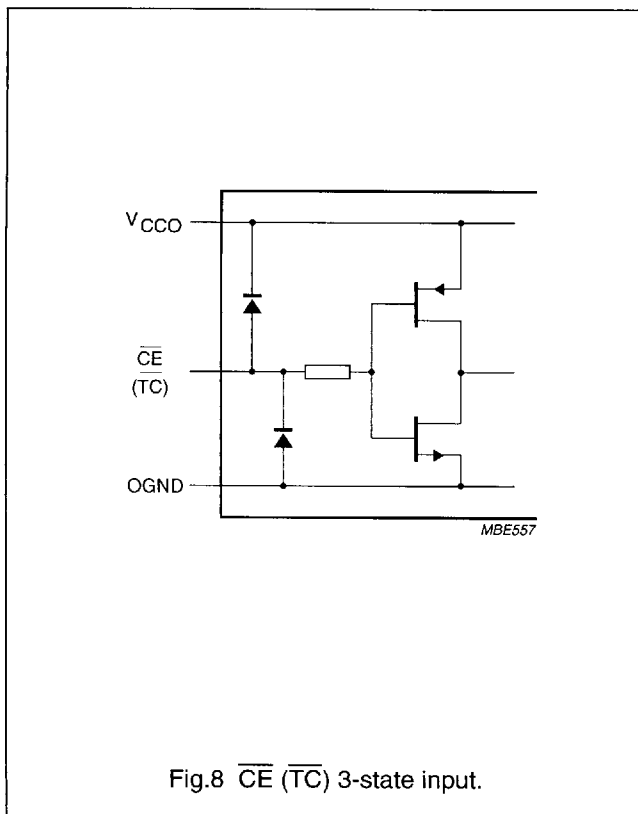


Fig.8  $\overline{CE}$  ( $\overline{TC}$ ) 3-state input.

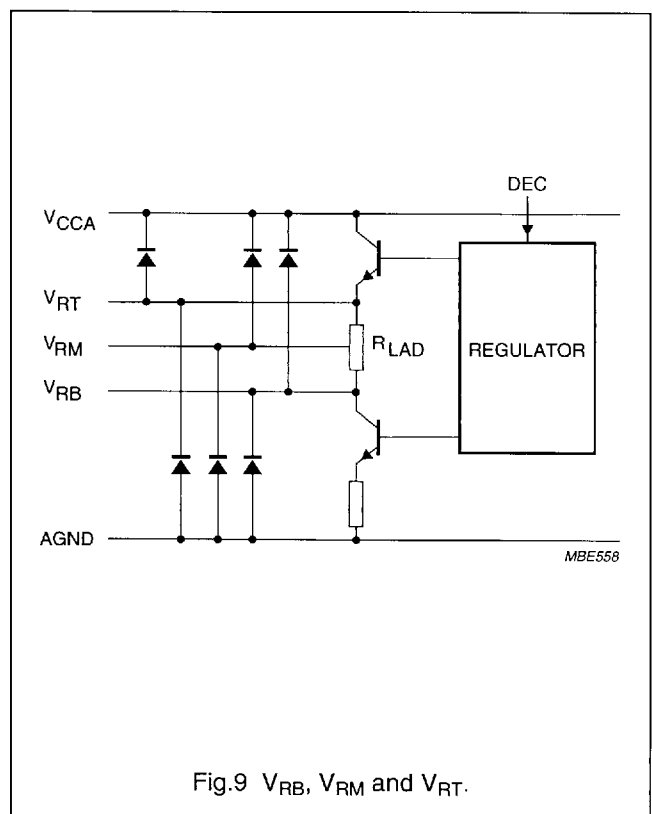


Fig.9  $V_{RB}$ ,  $V_{RM}$  and  $V_{RT}$ .

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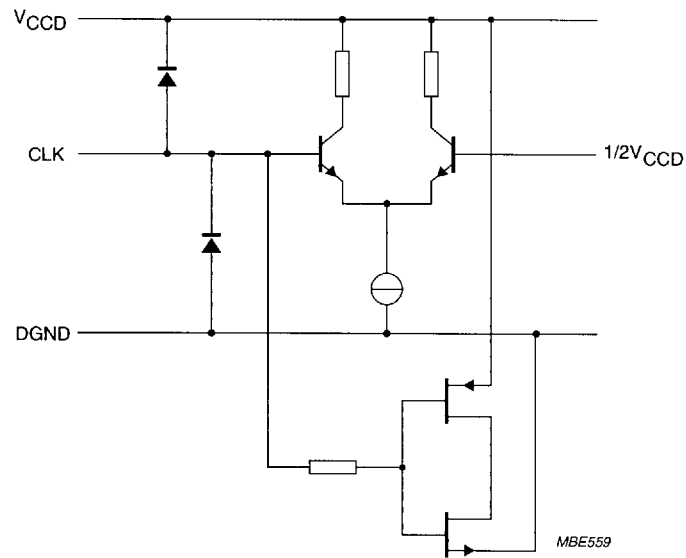
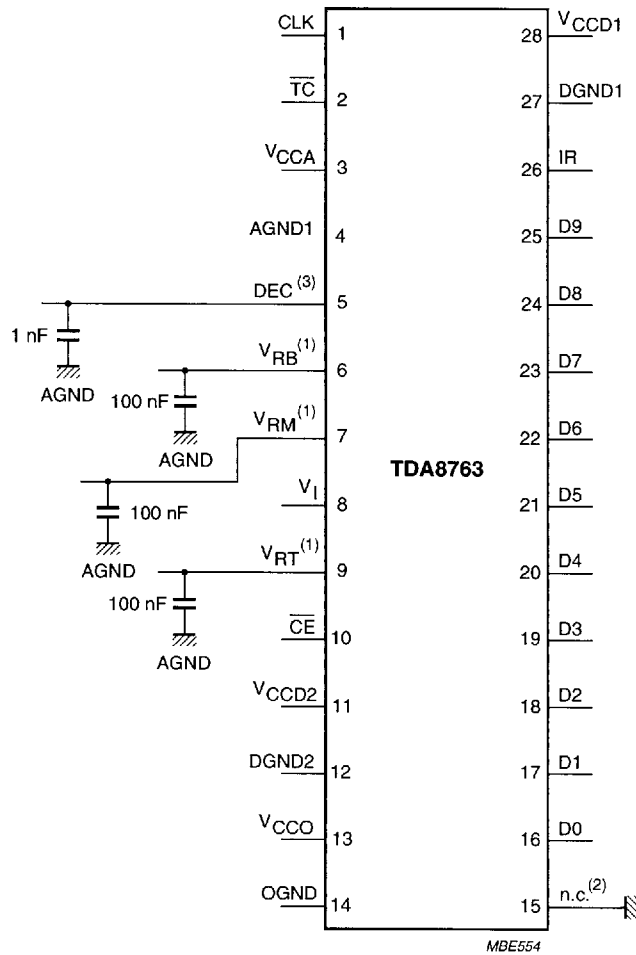


Fig.10 CLK input.

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APPLICATION INFORMATION



The analog and digital supplies should be separated and decoupled.

The external voltage generator must be built such that a good supply voltage ripple rejection is achieved with respect to the LSB value. Eventually, the reference ladder voltages can be derived from a well regulated  $V_{CCA}$  supply through a resistor bridge and a decoupled capacitor.

For applications where the input signal must remain well centred around middle scale,  $V_{RM}$  must be decoupled and connected to analog input signal (pin 8) through a resistor. The values must be defined in accordance with the input signal frequency in order to avoid direct coupling into the ADC ladder (e.g.  $R = 5\text{ k}\Omega$  and  $C = 100\text{ nF}$ ).

(1)  $V_{RB}$ ,  $V_{RM}$  and  $V_{RT}$  are decoupled to AGND

(2) Pin 15 should be connected to DGND in order to prevent noise influence.

(3) When pin 5 (DEC) is directly short-circuited to AGND, an external regulator can be connected to  $V_{RT}$  and  $V_{RB}$ .

Fig.11 Application diagram.

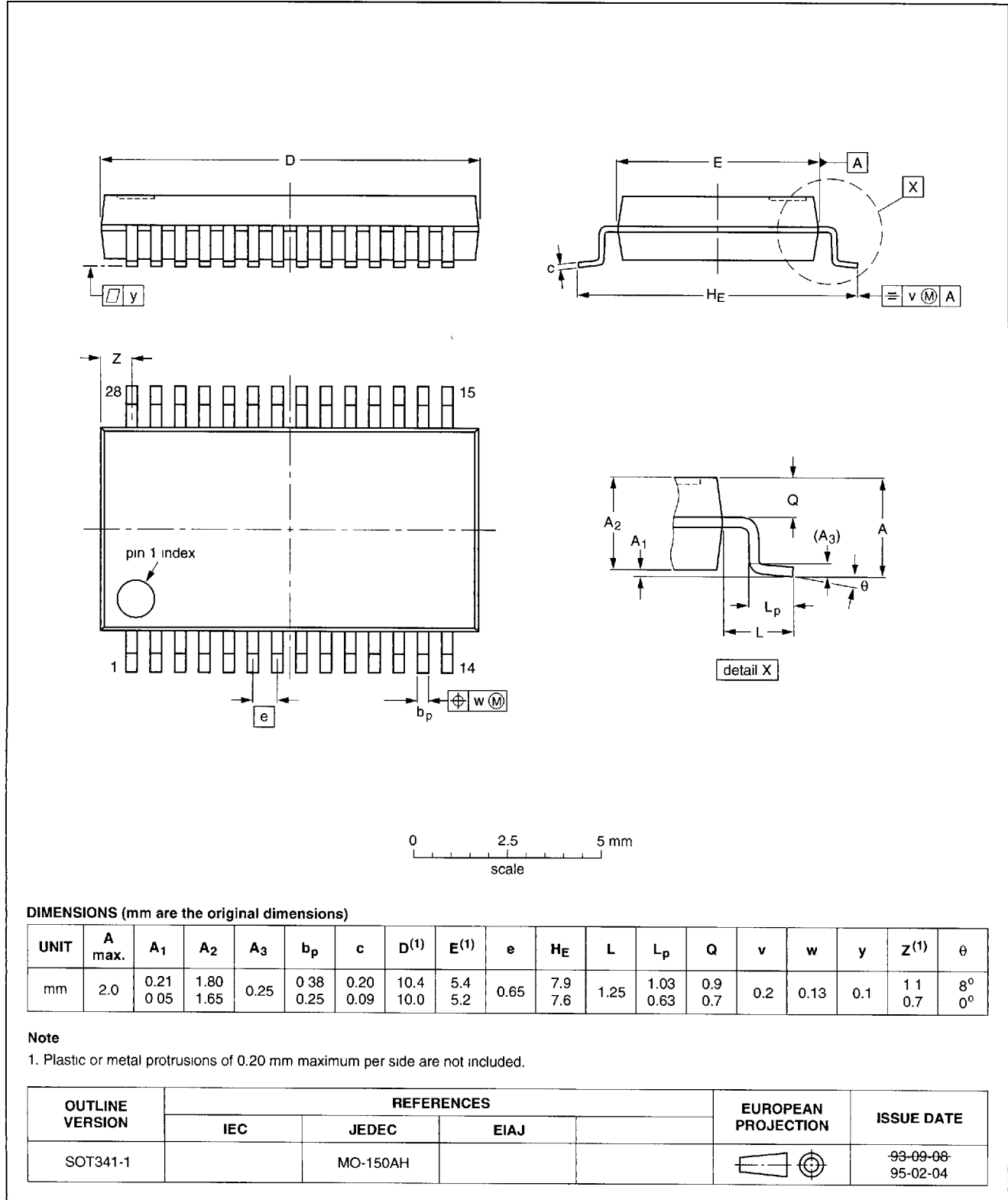
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PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm

SOT341-1





# 10-bit high-speed low-power analog-to-digital converter

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## SOLDERING SSOP

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C.